LISTING OF CLAIMS

Claims 1-8. (Canceled).

9. (Currently Amended) A memory circuit, comprising:

a data latch having a true latch node and a complement latch node; and

circuitry responsive to a control signal to short the true latch node to the complement latch node for the purpose of destroying data stored by the latch.

10. (Currently Amended) The circuit of claim 9 wherein the circuitry comprises a p-channel transistor having its conduction terminals connected between the true latch node and the complement latch node and its gate connected to receive the control signal.

11. (Currently Amended) The circuit of claim 9 wherein the circuitry comprises an n-channel transistor having its conduction terminals connected between the true latch node and the complement latch node and its gate connected to receive the control signal.

12. (Currently Amended) The circuit of claim 9 wherein the memory circuit further includes:

a first pass gate coupling the true latch node to a bit line;

a second pass gate coupling the complement latch node to a complement bit line.

13. (Original) The circuit of claim 12 wherein the data latch is coupled to a reference voltage line, further comprising a circuit which disconnects the reference voltage line from the latch when the control signal is activated.

14. (Currently Amended) A memory circuit, comprising:

a data latch having a true latch node and a complement latch node;

a first pass gate coupling the true latch node to a bit line;

a second pass gate coupling the complement latch node to a complement bit line; and

a logic circuit generating a logic control signal to simultaneously activate the first and second pass gates to short the true and complement latch nodes to the bit line and complement bit line, respectively, for the purpose of destroying data stored by the latch.

15. (Original) The circuit of claim 14 wherein the data latch is coupled to a reference voltage line, further comprising a circuit which grounds the reference voltage line when the logic circuit generates the logic control signal.

16. (Currently Amended) A memory circuit, comprising:

a data latch having a true latch node and a complement latch node;

circuitry responsive to a control signal to short one of the true/complement latch nodes of the latch to a reference voltage for the purpose of destroying data stored by the latch.

17. (Currently Amended) The circuit of claim 16 wherein the circuitry comprises an n-channel transistor having its conduction terminals connected between the one of the true/complement latch nodes and the reference voltage.

18. (Currently Amended) The circuit of claim 16 wherein the circuitry comprises a p-channel transistor having its conduction terminals connected between the one of the true/complement latch nodes and the reference voltage.

19. (Original) The circuit of claim 16 wherein the data latch is coupled to a reference voltage line, further comprising a circuit which disconnects the reference voltage line from the latch when the control signal is activated.

20. (Currently Amended) The circuit of claim 16 wherein the memory circuit further includes:

a first pass gate coupling the true latch node to a bit line;

a second pass gate coupling the complement latch node to a complement bit line.

21. (Currently Amended) A memory circuit, comprising:

a data latch having a true latch node and a complement latch node; and

circuitry responsive to at least one control signal to short both the true and complement latch nodes of the latch to at least one reference voltage for the purpose of destroying data stored by the latch.

22. (Currently Amended) The circuit of claim 21 wherein the circuitry comprises:

a first n-channel transistor having its conduction terminals connected between the true latch node and the reference voltage; and

a second n-channel transistor having its conduction terminals connected between the complement latch node and the reference voltage.

23. (Original) The circuit of claim 22 wherein the a gate of the first transistor and a gate of the second transistor receive the same control signal.

24. (Original) The circuit of claim 22 wherein the a gate of the first transistor and a gate of the second transistor receive the different control signals.

25. (Currently Amended) The circuit of claim 21 wherein the circuitry comprises:

a first p-channel transistor having its conduction terminals connected between the true latch node and the reference voltage; and

a second p-channel transistor having its conduction terminals connected between the complement latch node and the reference voltage.

26. (Currently Amended) The circuit of claim 25 wherein ~~the~~ a gate of the first transistor and a gate of the second transistor receive the same control signal.

27. (Currently Amended) The circuit of claim 25 wherein ~~the~~ a gate of the first transistor and a gate of the second transistor receive the different control signals.

28. (Currently Amended) The circuit of claim 21 wherein the circuitry comprises:

an n-channel transistor having its conduction terminals connected between one of the true/complement latch nodes and a first reference voltage; and

a p-channel transistor having its conduction terminals connected between the other of the true/complement latch nodes and a second reference voltage.

29. (Original) The circuit of claim 21 wherein the data latch is coupled to a reference voltage line, further comprising a circuit which disconnects the reference voltage line from the latch when the control signal is activated.

30. (Currently Amended) The circuit of claim 21 wherein the memory circuit further includes:

a first pass gate coupling the true latch node to a bit line;

a second pass gate coupling the complement latch node to a complement bit line.

Claims 31-34. (Canceled).

35. (Original) A memory circuit, comprising:

a memory cell including a data node;

a pass gate coupling the data node of the memory cell to a bit line; and

circuitry responsive to at least one control signal to short the bit line to a reference voltage while the pass gate is activated for the purpose of destroying data stored by the memory cell.

36. (Original) The circuit of claim 35 wherein the circuitry comprises a transistor having conduction terminals connecting the bit line to a reference voltage and a gate coupled to receive the at least one control signal.

37. (Original) The circuit of claim 35 wherein the circuitry comprises a first transistor having its conduction terminals connecting the bit line to a first reference voltage and a second transistor having its conduction terminals connecting the bit line to a second reference voltage, the first and second transistors each having a gate coupled to receive the at least one control signal.

38. (Original) The circuit of claim 35 further including a coupling circuit for selectively shorting the bit line to a word line to share charge therebetween.

39. (Original) The circuit of claim 38 further including a pull up device to pull the word line up to a positive reference voltage after charge has been shared between the bit line and word line.